1. (Withdrawn) A method for interconnecting an integrated circuit (IC) multiple die assembly to conductors on a substrate for conveying signals there between, wherein the multiple die assembly includes a base IC die having a surface and includes at least one secondary IC die mounted on the surface of the base IC die with signal paths provided therebetween, the method comprising the steps of:

a. providing conductive contacts on the surface of the base IC die, each conductive contact having a free end extending outward from the first surface beyond the secondary IC die; and

b. mounting the multiple die assembly on the substrate such that the free end of each contact is brought into contact with the conductors on the substrate and such that the secondary IC resides between the surface of the base IC die and the substrate, wherein the contacts convey the signals between the base IC die and the conductors on the substrate.

2. (Withdrawn) The method in accordance with claim 1 wherein step b further comprises soldering the free ends of the conductive contacts to the conductors on the substrate and the surface of the substrate.

3. (Withdrawn) The method in accordance with claim 1 wherein the conductive contacts are resilient spring contacts.

4. (Withdrawn) The method in accordance with claim 3 wherein step b comprises:

clamping the multiple die assembly to the substrate so that the spring contacts are compressed against the conductors on the surface of the substrate.

5. (Withdrawn) A method for fabricating and testing a multiple die assembly, the method comprising the steps of:

a. providing a substrate having conductors formed thereon;

b. providing a base IC wafer including at least one base IC die having a first surface and a second surface parallel to the first surface;

c. forming conductive contacts on the first surface of the IC die, each conductive contact having a free end extending outward from the first surface of the base die;

d. linking a first secondary IC die;

e. linking the first secondary IC die to the first surface of the base IC die through first conductive signal paths;

f. separating the base IC die from other portions of the base IC wafer; and

g. positioning the base IC die such that its first surface faces the substrate, such that free ends of the first conductive contacts contact the conductors on the substrate, and such that the first secondary IC die resides between the first surface of the base IC die and the substrate, wherein the conductive contacts convey signals between the base IC die and the conductors on the substrate.

6. (Withdrawn) The method in accordance with claim 5 wherein the conductive contacts are resilient spring contacts.

7. (Withdrawn) The method in accordance with claim 5 wherein the first conductive signal paths are formed by solder.

8. (Withdrawn) The method in accordance with claim 5, wherein step d comprises the substeps of:

d1. providing a secondary IC wafer having the secondary IC die formed thereon,

d2. testing the secondary IC die, and then

d3. cutting the secondary IC wafer to singulate the secondary IC die.

9. (Withdrawn) The method in accordance with claim 5, further comprising the step of:

n. prior to step 3, linking the base IC die through the conductive contacts to an apparatus for testing the base IC die.

10. (Withdrawn) The method in accordance with claim 5, further comprising the step of:

i. prior to step f, linking the multiple die assembly through the conductive contacts to an apparatus for testing the multiple die assembly.

11. (Withdrawn) The method in accordance with claim 9, further comprising the step of:

i. prior to step g, linking the multiple die assembly through the conductive contacts to an apparatus for testing the multiple die assembly.

12. (Withdrawn) The method in accordance with claim 5 further comprising the steps of:

h. providing a second secondary IC die;

i. linking the second secondary IC die to the second surface of the base IC die through second conductive signal paths.

13. (Withdrawn) The method in accordance with claim 12 further comprising the step of

j. forming conductive vias through the base IC wafer for providing signal paths between the first and second surfaces of the base IC die.

14. (Withdrawn) The method in accordance with claim 12 wherein the second conductive signal paths comprise spring contacts.

15. (Withdrawn) The method in accordance with claim ~~5~~ 12 wherein solder forms the second conductive signal paths.

16. (Withdrawn) The method in accordance with claim 5 wherein the substrate is a printed circuit board substrate.

17. (Withdrawn) The method in accordance with claim 5 wherein the substrate is a semiconductor substrate.

18. (Withdrawn) The method in accordance with claim 6 wherein the first conductive signal paths are formed by solder and wherein step d comprises the substeps of:

d1. providing a secondary IC wafer having the secondary IC die formed thereon,

d2. testing the secondary IC die, and then

d3 cutting the secondary IC wafer to singulate the secondary IC die.

19. (Withdrawn) The method in accordance with claim 18 further comprising the steps of:

h. prior to step e, linking the base IC die through the spring contacts to an apparatus for testing the base IC die, and

i. prior to step f, linking the multiple die assembly through the spring contacts to an apparatus for testing the multiple die assembly.

20. (Withdrawn) The method in accordance with claim 19 further comprising the steps of:

j. providing a second secondary IC die;

k. linking the second secondary IC die to the second surface of the base IC die through second conductive signal paths, and

l. forming conductive vias through the base IC wafer for providing signal paths between the first and second surfaces of the base IC die.

21. (Currently Amended) A multiple die electronic system comprising:

a substrate having conductors formed thereon,

a base IC die having a first surface facing the substrate and a second surface parallel to the first surface,

a first secondary IC die residing between the first surface of the base IC die and the substrate and linked to the first surface of the base IC die through first conductive signal paths,

conductive contacts extending between the first surface of the base IC die and the conductors on the substrate for conveying first signals between the base IC die and the conductors on the substrate, wherein at least one of second signals provided between the first secondary IC die and the base IC die has a higher frequency than the first signals provided between the base IC die and the substrate.

22. (Original) The multiple die electronic system in accordance with claim 21 wherein solder forms the first conductive signal paths.

23. (Original) The multiple die electronic system in accordance with claim 21 wherein the substrate is a printed circuit board substrate.

24. (Original) The multiple die electronic system in accordance with claim 21 wherein the substrate is a semiconductor substrate.

25. (Original) The multiple die electronic system in accordance with claim 21 wherein the conductive contacts comprise resilient spring contacts.

26. (Original) The multiple die electronic system in accordance with claim 25 wherein the spring contacts are formed on the first surface of the base IC die and soldered to the conductors on the substrate.

27. (Original) The multiple die electronic system in accordance with claim 21 wherein the conductive contacts comprise:

resilient spring contacts formed on the first surface of the base IC die, and a spring contact socket providing signal paths between the spring contacts and the conductors on the substrate.

28. (Currently Amended) ~~The~~ A multiple die electronic ~~system in accordance with claim 25 further~~ comprising:

a substrate having conductors formed thereon;

a base IC die having a first surface facing the substrate and a second surface parallel to the first surface;

a first secondary IC die residing between the first surface of the base IC die and the substrate and linked to the first surface of the base IC die through first conductive signal paths;

conductive contacts comprising resilient springs extending between the first surface of the base IC die and the conductors on the substrate for conveying signals between the base IC die and the conductors on the substrate; and

means for holding the base IC die proximate to the substrate so that the spring contacts are compressed against the conductors on the surface of the substrate.

29. (Currently Amended) ~~The~~ A multiple die electronic ~~system in accordance with claim 21 further~~ comprising:

a substrate having conductors formed thereon;

a base IC die having a first surface facing the substrate and a second surface parallel to the first surface;

a first secondary IC die residing between the first surface of the base IC die and the substrate and linked to the first surface of the base IC die through first conductive signal paths;

first conductive contacts extending between the first surface of the base IC die and the conductors on the substrate for conveying signals between the base IC die and the conductors on the substrate;

a second secondary IC die; and

second conductive paths linking the second secondary IC die to the second surface of the base IC die.

30. (Original) The multiple die electronic system in accordance with claim 29 further comprising:

conductive vias for providing signal paths between the first and second surfaces of the base IC die.

31. (Original) The multiple die electronic system in accordance with claim 29 wherein the second conductive paths comprise spring contacts.

32. (Withdrawn) A multiple die electronic system comprising:

a substrate having conductors formed thereon,

a base IC die having a first surface facing the substrate and a second surface parallel to the first surface,

a second level IC die having a third surface and residing between the first surface of the base IC die and the substrate and linked to the first surface of the base IC die and the substrate and linked to the first surface of the base IC die through first conductive contacts for conveying signals between the base IC die and the second level IC die,

a third level IC die residing between the first surface of the base IC die and the third surface of the second level IC die and linked to the third surface of the second level IC die through conductive signal paths, and

second conductive contacts extending between the first surface of the base IC die and the conductors on the substrate for conveying signals between the base IC die and the conductors on the substrate.

33. (Withdrawn) The multiple die electronic system in accordance with claim 32 wherein solder forms the conductive signal paths.

34. (Withdrawn) The multiple die electronic system in accordance with claim 32 wherein the substrate is a printed circuit board substrate.

35. (Withdrawn) The multiple die electronic system in accordance with claim 32 wherein the substrate is a semiconductor substrate.

36. (Withdrawn) The multiple die electronic system in accordance with claim 32 wherein the first and second conductive contacts comprise resilient first and second spring contacts.

37. (Withdrawn) The multiple die electronic system in accordance with claim 36 wherein the first spring contacts are formed on the first surface of the base IC die and soldered to the third surface of the second level IC die.

38. (Withdrawn) The multiple die electronic system in accordance with claim 36 wherein the second spring contacts are formed on the first surface of the base IC die and soldered to the conductors on the substrate.

39. (New) The multiple die electronic system in accordance with claim 21 further comprising:

a third level IC die residing between the first surface of the base IC die and a third surface of the first secondary IC die residing between the first surface of the base IC die and the substrate, the third level IC linked to the third surface of the second level IC die through conductive signal paths.